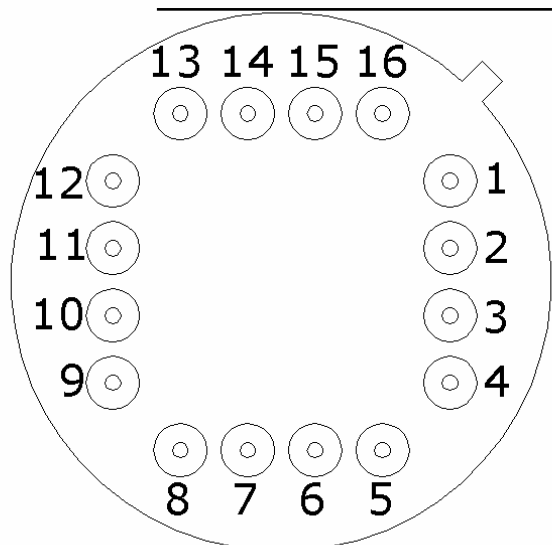


Bottom

2



Connect all reference voltages via
100 nF capacitors to VSS.

Pin Assignment

Pin	Name	Description	Type
1	VSS	Negative power supply voltage	Power
2	CONT	Control Pin for SPI	Digital Input
3	OUT_A	Analog Output	Analog Output
4	VCM_C	Common mode voltage	Reference Voltage*
5	VCM_OUT	Common mode voltage	Reference Voltage*
6	VREF_N	Negative reference voltage for ADC	Reference Voltage*
7	VREF_P	Positive reference voltage for ADC	Reference Voltage*
8	VREF_1225V	1.225V reference voltage	Reference Voltage*
9	AGND	Analog ground for ADC	Reference Voltage*
10	VDDA	Positive power supply voltage	Power
11	VDD	Positive power supply voltage	Power
12	POR_N	Power on reset, negatived	Digital Input
13	CLK_1MHZ	Master clock	Digital Input
14	VSAM	Valid sample	Digital Output
15	SCLK_IO	Clock input/output for SPI	Digital Input/Output
16	DATA_IO	Data input/output for SPI	Digital Input/Output

*) Connect via 100 nF to VSS

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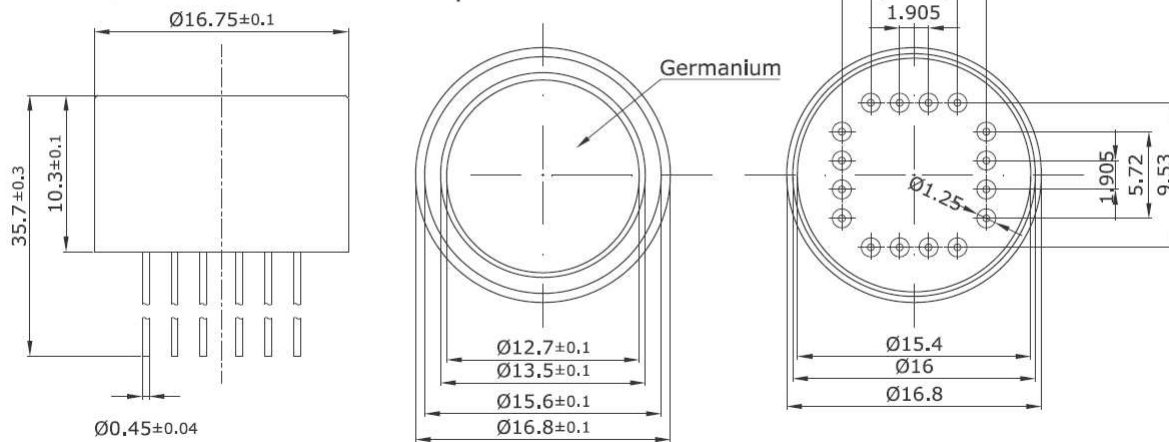
Array with Ge-Lens L=7mm

Bottom

3

Sideview

Top

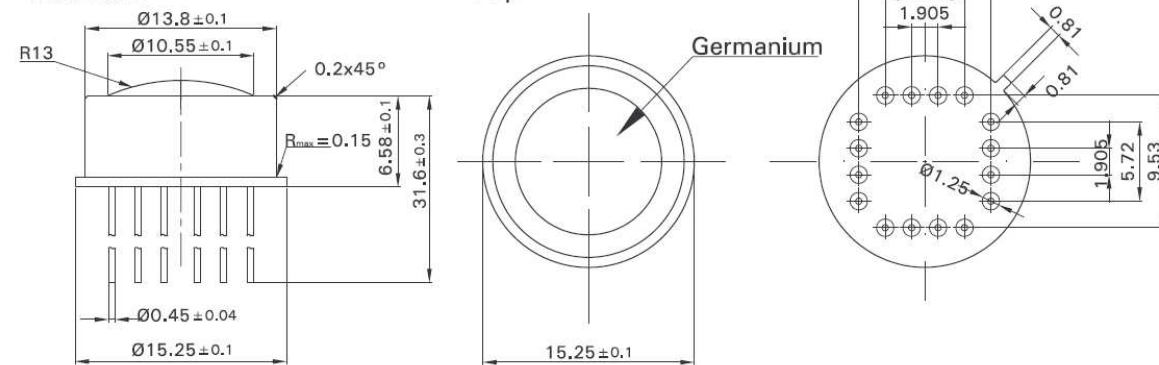


Array with Ge-Lens L = 4mm

Bottom

Sideview

Top



Internal Register Map:

Num	Name	Function	Default	Notes
0	R	Reset	0	In case of 1, the mux pixel counter is reset.
1	OPCTL	Operating point control low	1	00: Analog operating point is at start of AD-range, only positive signals are convertible 01: Analog operating point is in the middle of AD-range, positive and negative signals are convertible 10: Analog operating point is at end of AD-range, only negative signals are convertible
2	OPCTLH	Operating point control high	0	11:00
3	MA0	Multiplexer address 0	0	
4	MA1	Multiplexer address 1	0	
5	MA2	Multiplexer address 2	0	
6	MA3	Multiplexer address 3	0	-not used- write '0' to this location
7	MA4	Multiplexer address 4	0	-not used- write '0' to this location
8	MA5	Multiplexer address 5	0	-not used- write '0' to this location
9	MA6	Multiplexer address 6	0	-not used- write '0' to this location
10	AIM	Automatic increment mode	1	1 : auto increment mode 0: manual mode (the pixel selected by following Multiplexer address)
11	AMPL	Amplification low bit	0	0: low amplification 1: high amplification
12		spare	0	-not used- write '0' to this location
13		spare	0	-not used- write '0' to this location
14		spare	0	-not used- write '0' to this location
15	BDUR	Break Duration	0	0: 64clks of MCLK 1: 32clks of MCLK

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Characteristics:

Common Specifications:

• Number of Thermocouples	80
• Technology	n-poly/p-poly Si
• Element Resistance	approx. 80 kOhms
• Sensitivity	approx. 60 V/W without optics and filter
• Thermal Pixeltime constant	<4 ms
• MUX preamplifier noise	approx. 30 nV/ $\sqrt{\text{Hz}}$
• Internal ADC	12 bit
• Digital Interface	SPI
• Analog Output	Yes
• 2 point selectable Gains	2640x / 7920 x

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Array-dependent Specifications:

9x8 elements:

- Pitch 300 μm
- Absorber size 220 μm
- Max. Framerate 66,8 Hz
(without Averaging)
- 4 internal Amps + MUX
- 64 sensitive elements

17x16 elements:

- Pitch 220 μm
- Absorber size 130 μm
- Max. Framerate 17,7 Hz
(without Averaging)
- 8 internal Amps + MUX
- 256 sensitive elements

FOV(L=3mm)= 43.6 deg

FOV(L=4mm)= 33.4 deg

FOV(L=7mm)= 19.5 deg

FOV(L=3mm)= 60.8 deg

FOV(L=4mm)= 47.5 deg

FOV(L=7mm)= 28.2 deg

L equals the focal length of the lens.

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Electric Specifications:

Absolute Maximum Ratings:

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V _{CC}		-0.5		6	V
Voltage at All inputs and outputs	V _{IO}		-0.5		V _{CC} +0.5	V
Storage Temperature	T _{STG}		-30		125	Deg. C

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Operating Conditions:

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V _{CC}		4.5		5.5	V
Operation Temperature	T _A		0		85	Deg. C
ESD-Protection		Human body model	1.5			kV
		100pF + 1k50hm				

Electrical Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
-----------	--------	-----------	------	------	------	------

Digital Input

Frequency of MCLK	MCLK			1M	TBD	Hz
Input voltage high	V _{IH}		V _{dd} -1.2			V
Input voltage low	V _{IL}				1.2	V
Operating Frequency	f _{OP}	CLK_1MHz	500k	1M	TBD	Hz

PTAT

Temperature range			0		85	Deg. C
PTAT value@ -20°C				TBD		V
PTAT value@100°C				TBD		V

Signal Processing

First amplifier stage gain	G0		TBD	880	TBD	V/V
Second amplifier stage gain	G1	AMPL=0	TBD	3	TBD	V/V
Second amplifier stage gain	G1	AMPL=1	TBD	9	TBD	V/V
Analog path Output ripple	V _{PPSENS}		-	-	TBD	mV
Temp. coefficient Thermopile path output voltage	TCO _{OUTA}		TBD	-	TBD	mV/K

VoltageReference

VREF_1225	V _{REF}	V _{CC} =5V, T _{amb} =25°C	1.2	1.225	1.25	V
Temp. coeff. of V _{REF}	TC _{REF}		TBD		TBD	ppm/K

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Analog Output

Output voltage swing	V_{OUTA}	load 10kOhm	0.5		$V_{CC}-0.8$	V
Power supply rejection ratio	P_{SRR}	AMPL=1	TBD			dB
Output current limit	I_{OUTA}	OUT_A	0.15			mA

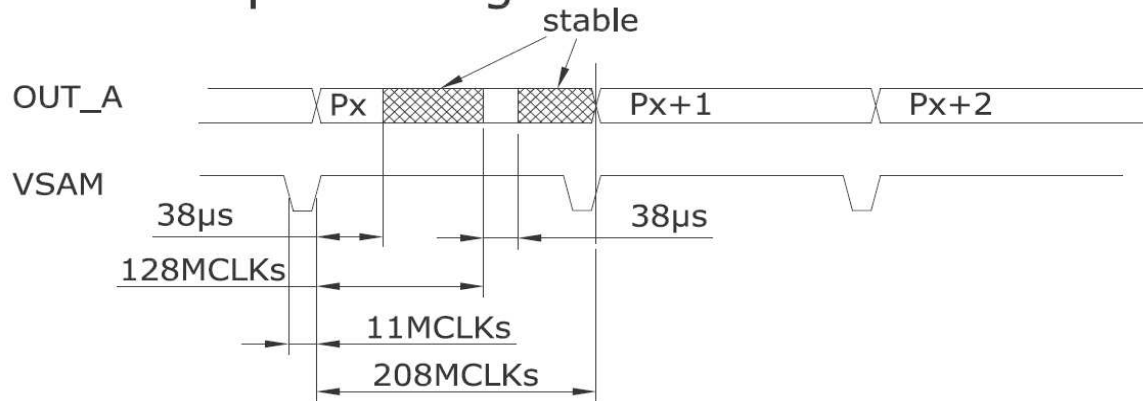
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General Parameters

Overall current consumption	I_{DD}	CLK_1MHz=1MHz		TBD	TBD	mA
Start up time	T_{POR}	CLK_1MHz=1MHz Power On to first sample			TBD	mS

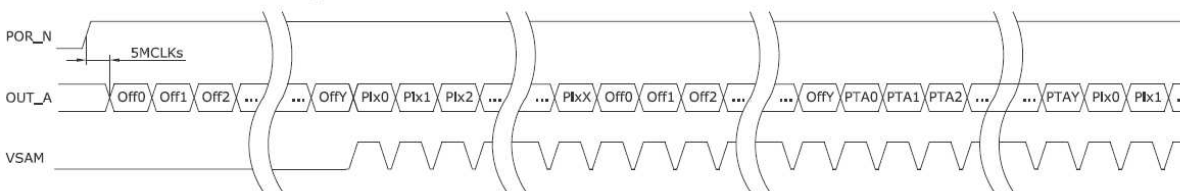
Timings

Sample Timing



Every analog voltage has 2 stable domains, as shown above.

Serial Transmission of analogue data



Off0...OffY Electric offset of amplifier 0 to amplifier Y
Pix0...PixX Amplified pixel voltage of Pixel0 to PixelX
PTA0...PTAY PTAT-Signal (Y-times)

Constants for array types:

Type 8x9: Type 16x17:
Y=3 Y=7
X=63 X=255

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SPI Communication:

Data sampled at rising edge of SCLK, MSB first.

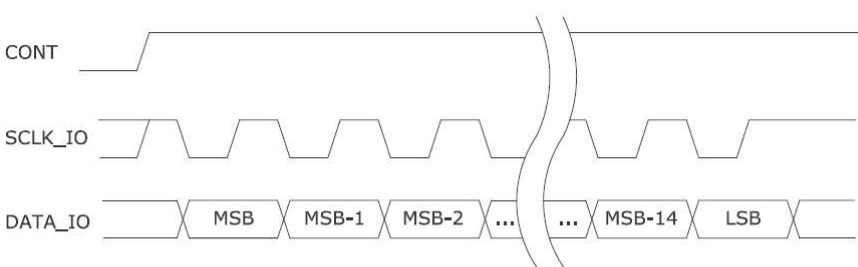
In case of ASIC as master device the frequency of the SCLK_IO is equal to the frequency of MCLK/2. The three MSB's signify the row-address of the current pixel, the other bits describe the ADC-result.

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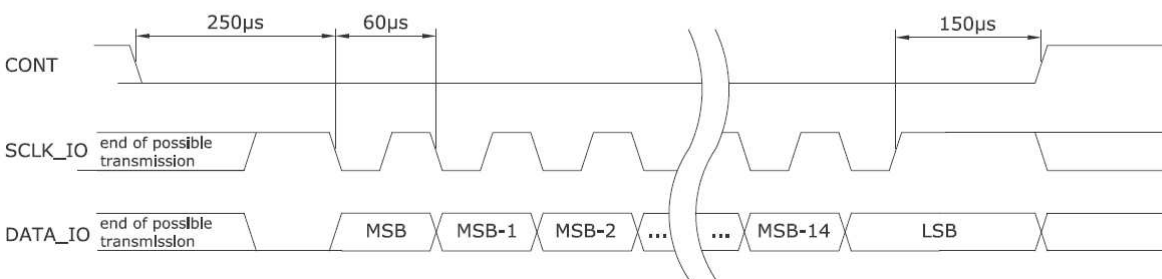
The output drivers for SCLK_IO and DATA_IO are enabled by CONT.

If CONT is low the data can be written serially from external controller through DATA_IO. In that case the external controller has to wait a minimum delay time, until SCLK_IO and DATA_IO output drivers are disabled. After programming, the positive slope of CONT stores the contents, when the number of SCLK-pulses is equal 16. While the output driver of the ASIC is disabled a weak pull up ensures that the SCLK_IO pin is at high level. To execute a reset command, the μ C has to write a logical "1" to the R-Bit in to configuration and afterwards a "0" into the R-bit, which requires two write cycles in this special case.

Serial Read from ASIC



Serial Write to ASIC



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